PATENT
8733.289.00

UNITED STATES PATENT APPLICATION

OF

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FOR

LIQUID CRYSTAL DISPLAY AND DRIVING METHOD THEREOF

This application claims the benefit of Korean Patent Application No. 2000-36648, filed on June 29, 2000, which is hereby incorporated by reference.

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a liquid crystal display, and more particularly to a liquid crystal display device and a driving method thereof that is adaptive for restraining a generation of a transient current.

Discussion of the Related Art

Generally, a liquid crystal display device has an inherent resolution corresponding to the number of integrated pixels, and has a higher resolution as its dimension becomes larger. In order to display a high quality of picture, makers of the liquid crystal display device increase a pixel integration ratio within a liquid crystal panel between liquid crystal display devices with same dimension to differentiate the resolution.

In the liquid crystal display device, a data clock DCLK according to the XGA class data is 65MHz on the basis of a refresh rate of 60Hz. More specifically, in a system including a video card, a frequency of the data clock DCLK transferred to the liquid crystal display device is 65MHz at a XGA resolution; 108MHz at a SXGA resolution; and 160MHz at a UXGA resolution.

In the liquid crystal display (LCD) as mentioned above, a frequency of an accepted input data clock of driver integrated circuits for displaying a data on a liquid crystal display panel is about 45 to 60MHz. Accordingly, the recent liquid crystal display device divides input and output data in parallel so as to reduce a high data clock frequency and

transfers the data simultaneously over a plurality of transmission lines, thereby reducing driving frequencies of the driver integrated circuits.

Fig. 1 is a block diagram showing a configuration of the conventional LCD, which illustrates a LCD having a XGA class resolution. In recent, in order to reduce a frequency of a driving clock in the LCD, a data for two pixels divided into odd and even pixel data is inputted, via an interface, from the system. Thus, a frequency of the data clock DCLK is 35.5MHz lower than 65MHz which is a data clock frequency of an original image signal.

Referring to Fig. 1, a timing controller 10 receives odd and even data and a data clock from an interface (not shown). The timing controller 10 is synchronized with the data clock to supply a data driving circuit 20 including n data driver IC′ s D1 to Dn with the odd and even data. Then, the data driving circuit 20 supplies a liquid crystal display panel 30 with the odd and even data. At this time, a gate driving circuit 40 including m gate driver IC′ s G1 to Gm is synchronized with the odd and even data so that the liquid crystal display panel 30 may display a picture, thereby applying a pulse signal to the liquid crystal display panel 30. The data driver IC′ s D1 to Dn receives a source sampling signal from the timing controller 10 to latch a data.

Fig. 2 is a timing chart showing a frequency-division concept of a data clock (DCLK) frequency. Referring to Fig. 2, an original data (b) for one pixel is outputted in synchronization with a data clock DCLK1 (a). Then, the system or the LCD latches the data (b) to synchronize an odd data (d) and even data (e) with twice-frequency-divided data clock DCLK (c) and output the same simultaneously. Such a driving method is referred to as "two-port driving method" or "six-bus driving method" because the data (d) and (e) for two pixels

are simultaneously outputted, which has been disclosed in Korea Patent Application No. 95-19513 filed on July 4, 1995 by the same applicant.

However, the above-mentioned conventional LCD and driving method thereof reduces a driving frequency in the LCD, but increases a data amount outputted simultaneously according to an increase in a data output. For instance, in the case of a two-port driving method in the LCD using a 8-bit data, a data is simultaneously outputted, via 48 bit lines (i.e., 48 bit line = 2(port) X 3(R,G,B) X 8(bit)), from the timing controller 10. At this time, a transient current is generated within the timing controller 10 in a conversion process between data (high/low).

Recently, a high-resolution LCD capable of a high-resolution picture in a same size of LCD has been required to display a high quality picture. For instance, a data clock frequency in a high-resolution UXGA system is about 160MHz. An apparatus and method in Fig. 1 according to the conventional "two-port driving method" for reducing the data clock frequency is capable of reducing a data clock into about 80MHz. Since the above-mentioned data clock is higher than an accepted input value in the general diver IC's, however, a frequency reduction according to a high resolution has been more required. Accordingly, another conventional apparatus and method latches a data inputted with being divided into odd and even data one line by one line using a line memory and outputs 4 pixel data simultaneously according to a division of the panel area. Such a driving method may be referred to as "four-port driving method.

Fig. 3 is an operational timing chart according to the above-mentioned conventional four-port data transmission method. In Fig. 3, as an example, n driver IC's connected to the liquid crystal display panel 30 are two-division driven into left and right

groups as shown in Fig. 2. More specifically, data data1 to data1024 for one horizontal line inputted as shown in (b) and (c) in Fig. 3 are latched, and 4 pixel data are simultaneously outputted as shown in (e), (f), (g) and (h) in Fig. 3 upon inputting of the next horizontal line data. Accordingly, an input data clock (a) has a frequency reduced to 1/2 like a two frequency-divided source sampling clock SSC (d).

Assuming that an LCD according to the above-mentioned driving method uses a 8-bit data as an example, an output data line of the timing controller 10 becomes 4 X 3(R,G,B) X 8(bit) = 96 bit line. Thus, when the nth four data are converted and outputted to the (n+1)th four data, a transient current is generated within the timing controller 10. More specifically, when a data conversion of Low/High or High/Low is made, or when a plurality of data conversion of Low/High is made, a transient current flows in the timing controller 10.

Such a transient current shortens a life of the LCD and makes an adverse effect to devices such as a DC to DC converter (not shown) for a current supply, and generates an analog power noise, etc. Furthermore, the conventional LCD additionally requires a capacitor for eliminating the transient current to cause a complex configuration and a cost rise.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a liquid crystal display device wherein an output timing of a plurality of picture data in the LCD device is set differently to restrain a generation of transient current.

A further object of the present invention is to provide a driving method for an liquid crystal display device that is capable of reducing a generation of transient current according to a plurality of picture data output.

Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

In order to achieve these and other objects of the invention, a liquid crystal display device according to an aspect of the present invention includes a line memory for dividing a data for at least one line inputted from the exterior thereof into a plurality of groups to store the divided data therein and for outputting the data at a desired unit from each of the groups; a driving circuit including n driver integrated circuits(wherein n is an integer) that are connected to the line memory and a liquid crystal display panel to drive the liquid crystal display panel in response to the data outputted from the line memory; and a timing controller, being connected to the line memory and the driving circuit, for receiving a data clock inputted from the exterior thereof to output the data from the plurality of groups of said line memory to the driving circuit every period of the data clock in response to a time corresponding to the number of said groups.

A liquid crystal display device according to another aspect of the present invention includes a line memory for dividing a data for at least one line inputted from the exterior thereof into a plurality of groups to store the divided data therein and for outputting the data at a desired unit from each of the groups; a driving circuit including n driver

integrated circuits(wherein n is an integer) that are connected to the line memory and a liquid crystal display panel to drive the liquid crystal display panel in response to the data outputted from the line memory; and a timing controller, being connected to the line memory and the driving circuit, for receiving a data clock inputted from the exterior thereof to generate a first data clock by frequency-dividing the data clock at a frequency-division ratio corresponding to the number of said divided groups, and for outputting the data in each of the groups to the driving circuit during each period of the first data clock.

A liquid crystal display device according to still another aspect of the present invention includes a line memory for receiving two pixel data unit sequentially from the exterior thereof and dividing the data for at least one line into a plurality of groups to store the divided data therein and for outputting the two pixel data unit from each of the groups; a driving circuit including n driver integrated circuits(wherein n is an integer) that are connected to the line memory and a liquid crystal display panel to drive the liquid crystal display panel in response to the data outputted from the line memory; and a timing controller, being connected to the line memory and the driving circuit, for receiving a data clock inputted from the exterior thereof to generate a first data clock by frequency-dividing the data clock at a frequency-division ratio corresponding to the number of said divided groups, and for outputting the two pixel data in each of the groups to the driving circuit during each period of the first data clock.

A liquid crystal display device according to still another aspect of the present invention includes a latch circuit for latching and outputting two pixel unit inputted from the exterior thereof; a driving circuit including n driver integrated circuits(wherein n is an integer) that are connected to the latch circuit and a liquid crystal display panel to drive the

liquid crystal display panel in response to the data outputted from the latch; and a timing controller, being connected to the latch circuit and the driving circuit, for receiving a data clock inputted from the exterior thereof to output each one pixel data to the driving circuit at a desired time interval during one period of the data clock.

A method of driving A liquid crystal display device according to still another aspect of the present invention includes a data storage step of dividing and storing an input data for at least one line a plurality of groups; a data clock generating step of frequency-dividing an input first data clock at a frequency-division ratio corresponding to the number of said divided groups to generate a second data clock; a data outputting step of outputting a desired data unit from each of said groups at a different time during one period of the second data clock; and a displaying step of latching the output data for one line unit to drive a liquid crystal display panel in response to the latched data.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWING

The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention.

In the drawings:

FIG. 1 is a block diagram showing a configuration of a general liquid crystal display device;

FIG. 2 is an input and output timing chart of the liquid crystal display device of six-bus driving system shown in Fig. 1;

FIG. 3 is an operational timing chart according to the conventional four-port data transmission method;

FIG. 4 is a block diagram showing a configuration of a liquid crystal display device according to an embodiment of the present invention;

FIG. 5 is a block diagram showing a configuration of the line memory integrated to the timing controller in Fig. 4;

FIG. 6 is waveform diagrams for showing an operation timing according to an embodiment of the present invention; and

FIG. 7 is waveform diagrams for showing an operation timing according to another embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made in detail to the preferred embodiment of the present invention, example of which is illustrated in the accompanying drawings.

Referring to Fig. 4, there is shown a liquid crystal display (LCD) according to an embodiment of the present invention. In Fig. 4, a timing controller 410 stores odd and even data inputted from an interface (not shown) in a line memory 420. The line memory 420 consists of a first line memory block 411 and a second line memory block 416 as shown in Fig. 5. Assuming that a liquid crystal display panel 430 has been divided into left and right areas, the first line memory 411 includes a first odd memory block 412 for storing odd-numbered data in 1st to 512th pixels, a first even memory block 413 for storing even-

numbered data in 1st to 512th pixels, a second odd memory block 414 for storing odd-numbered data in 513th to 1024th pixels, and a second even memory block 415 for storing even-numbered data in 513th to 1024th pixels. The second line memory block 416 has a configuration similar to the first line memory block 411.

The first line memory block 411 divides data for one horizontal line into left and right areas in response to a read/write control signal of the timing controller 410 to store the same in the first odd and even memory blocks 412 and 413 and the second memory blocks 414 and 415, respectively. When the data storage in the first line memory block 411 has been completed, the next line data is divided into left and right areas and stored in the second line memory block 416. When the second memory block 416 is storing the data, the timing controller 410 is synchronized with the falling edge of a second source sampling clock SSC2 shown in (e) of Fig. 6 from the first line memory block 411 to output the odd and even data 513 and 514 shown in (f) and (g) of Fig. 6 from the second odd and even memory blocks 414 and 415, respectively, to a right data driver IC group D6 to D10. Then, the timing controller 410 is synchronized with the falling edge of a first source sampling clock SSC1 shown in (b) of Fig. 6 from the first line memory block 411 to sequentially output the odd and even data 1 and 2 shown in (c) and (d) of Fig. 6 from the first odd and even memory blocks 412 and 413, respectively, to a left data driver IC group D1 to D5. In other words, two pixel data are alternately synchronized with the first source sampling clock SSC1 and the second sampling clock SSC2, respectively, and are outputted from the first odd and even memory blocks 412 and 413 and the second odd and even memory blocks 414 and 415 at a timing having a difference of 1/2 period from each other. At this time, the first and second

source sampling clocks SSC1 and SSC2 have a frequency frequency-divided twice from a data clock DCLK shown (a) of Fig. 6.

Consequently, the timing controller 410 has a frequency reduced to 1/2 in comparison to that of the input data clock, generates the first and second source sampling clocks SSC1 and SSC2 having a phase contrary to each other. The timing controller 410 is synchronized with the first and second source sampling clocks SSC1 and SSC2 to sequentially output four pixel data to the left and right data driver IC groups connected to the left and right areas of the liquid crystal panel at a time difference of 1/2 period for each of the two pixel data.

Accordingly, the LCD according to an embodiment of the present invention drives the data driver IC's at a clock having a frequency reduced to 1/2 in comparison to that of the input data clock. Since the timing controller 410 outputs only each of the two pixel data simultaneously, it can not only reduce a driving frequency, but also restrain a generation of a transient current caused by a lot of data outputs. In other words, the LCD according to the present invention reduces a driving frequency using the four-port driving method to output only 48 bits which is equal to a half of 96 bit outputs in the prior art, so that it can restrain a generation of transient current.

In the above-mentioned embodiment of the present invention, the right data is outputted earlier, but the left data may be outputted earlier. Also, the first source sampling clock SS1 and the second source sampling clock SS2 has a delay time of 1/2 period from each other, but may have a delay time of 1/4, 3/4 and so on. Further, Fig. 4 to Fig. 6 have illustrated the four-port driving method reducing an operation frequency to 1/2 as an example, but it is possible to divide the liquid crystal panel into four areas and output the 8

pixels for each of four pixel data at a time difference of 1/2 period or output the 8 pixels for each of two pixel data at a time difference of 1/4 period so as to reduce an operation frequency to 1/4 as another embodiment. The embodiment described in Fig. 4 to Fig. 6 divides the liquid crystal panel into the left and right areas, it is possible to divide the data driver IC's into the odd and even groups D1, D3, ..., D9 and D2, D4, ..., D10. In addition, it is possible to divide the data lines into groups of even and odd numbers, etc. by arranging the data driver IC's at the upper and lower portions of the panel.

Moreover, the present invention is applicable to a case where it is not intended to reduce a driving frequency. Such another embodiment of the present invention will be described in detail with reference to Fig. 7.

In Fig. 7, a data clock DCLK ((a) of Fig. 7), a first sampling clock SSC1 ((d) of Fig. 7) and a second source sampling clock SSC2 ((f) of Fig. 7) has an equal frequency from each other. Also, a transfer rate of an input data is equal to that of an output data. First, the timing controller 410 generates the first source sampling clock SSC1 and the second source sampling clock SSC2 that have a frequency identical to the input data clock DCLK and a phase contrary to each other. Then, the timing controller 410 receives odd data d2n-1 ((b) of Fig. 7) and even data D2n ((c) of Fig. 7) at two ports. The timing controller 410 is synchronized with the rising edge of the first sampling clock SSC1 to output even data D2n-1 ((e) of Fig. 7). Also, the timing controller 410 is synchronized with the rising edge of the second sampling clock SSC2 to output even data D2n ((g) of Fig. 7) at a time difference of a 1/2 period in the data clock DCLK from an output time of the odd data D2n-1 shown in (e) of Fig. 7. According to the above-mentioned driving method, the line memory 420 for two lines is not required within the timing controller 410, but a latch circuit for latching at least two

pixels only is required. As a result, the above-mentioned another embodiment of the present invention uses the two-port driving method, but can output only each of 24 bits simultaneously.

As described above, according to the present invention, the driving frequency and the simultaneously outputted data amount are reduced to restrain a generation of transient current. Also, the simultaneously outputted data amount is reduced in spite of using the same driving frequency to restrain a generation of transient current. Accordingly, a capacitor configuration for eliminating a transient current can be omitted to reduce a manufacturing cost.

It will be apparent to those skilled in the art that various modifications and variation can be made in the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.